ANALYSIS AND MODELING OF PARASITIC CAPACITANCES IN ADVANCED NANOSCALE DEVICES

A Thesis

by

PRASANNA BEKAL

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2012

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Weiping Shi
Committee Members,	Peng Li
	Vivek Sarin
Head of Department,	Costas N. Georghiades

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ABSTRACT

Analysis and Modeling of Parasitic Capacitances in Advanced Nanoscale Devices.

(May 2012)

Prasanna Bekal, B.Tech., National Institute of Technology Karnataka, India

Chair of Advisory Committee: Dr. Weiping Shi

In order to correctly perform circuit simulation, it is crucial that parasitic capacitances near devices are accurately extracted and are consistent with the SPICE models. Although 3D device simulation can be used to extract such parasitics, it is expensive and does not consider the effects of nearby interconnect and devices in a layout. Conventional rule-based layout parasitic extraction (LPE) tools which are used for interconnect extraction are inaccurate in modeling 3D effects near devices. In this thesis, we propose a methodology which combines 3D field solver based extraction with the ability to exclude specific parasitics from among the parameters in the SPICE model. We use this methodology to extract parasitics due to fringing fields and sidewall capacitances in MOSFETs, bipolar transistors and FinFETs in advanced process nodes. We analyze the importance of considering layout and process variables in device extraction by comparing with standard SPICE models. The results are validated by circuit simulation using predictive technology models and test chips. We also demonstrate the versatility of this flow by modeling the capacitance contributions of the raised gate profile in nanoscale FinFETs.

To my parents

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Weiping Shi for giving me the opportunity to work under his guidance. I am very grateful to him for his constant encouragement and support over the duration of this project. The discussions and meetings that I have had with him have been a great source of knowledge and inspiration. I would also like to thank him for enabling access to the design tools, facilities and the constant support over the course of this research.

I would like to thank my committee members, Dr. Peng Li and Dr. Vivek Sarin. Special thanks to Jorge Edgar-Zarate from the Analog & Mixed Signal group for his assistance with the benchmark circuits and his valuable feedback.

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CHAPTER I

INTRODUCTION

As devices like FinFETs and bipolar junction transistors (BJT) are scaled down to nanometer dimensions, parasitic capacitances play an important role in controlling their performance [1]. Hence in order to get accurate feedback on circuit performance from SPICE, it is crucial that these devices are subject to a robust modeling procedure. Conventional rule-based LPE tools can be used to analyze intrinsic and coupling parasitic capacitances in devices and circuits. However, they are insufficient to model fringing fields in complex 3D geometry near device layers [2]. Numerical device simulations are often employed to overcome this limitation and the resulting models are provided to SPICE simulators through BSIM models [3]. Thus a careful study of parameters included in SPICE models is necessary to avoid double counting of parasitics extracted using extraction tools. For MOSFET devices, the treatment of parasitic near devices is well understood and standard options are available in commercial parasitic extraction tools [4] and foundries. However for FinFETs and advanced bipolar devices, there is no standard treatment available. Circuit designers often try by error on what parasitics to include and what to exclude. This is the first study, to the best of our knowledge, on how to correctly model parasitic near bipolar devices. We hope it will lead to better understanding on this problem and standardization.

Our work focuses on analyzing the parasitic capacitance component due to

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This thesis follows the style of *IEEE Transactions on Automatic Control*.

fringing fields in MOSFETs, double polysilicon self-aligned BJTs and FinFETs. As an alternative to using device simulators and previously developed models, we use a 3D field solver based extraction tool by Mentor Graphics to characterize this component quickly and accurately. We discuss the advantages of using this approach compared to the others.

A 3D field solver utilizes sophisticated computational algorithms using Finite Difference Method to characterize capacitances adjacent to complex devices [5]. The methodology developed uses the Calibre set of tools by Mentor Graphics to process the GDS layouts, netlists and process technology information from the foundry. We have also demonstrated that our method can be applied to other types of devices like CMOS and FinFETs. Other components of device parasitics like fringing field capacitances and via/contact capacitances have also been analyzed in order to ascertain the impact of scaling.

The remainder of the thesis is organized as follows. In Chapter II the proposed methodology is described along with a flowchart. In Chapter III the methodology is tested for a basic MOSFET and the results compared with existing models. In Chapter IV a new model for sidewall fringing capacitance is proposed for BJT and analyzed using a benchmark circuit. In Chapter V a more detailed modeling is performed for FinFET devices and the results are presented. Finally, the conclusions are presented in Chapter VI.

CHAPTER II

METHODOLOGY DEVELOPMENT

We utilize the Calibre suite of tools by Mentor Graphics to develop a methodology which enables parasitic extraction of devices and cells to a very high degree of accuracy. A range of scripts were developed in order to exercise control over the types of parasitics being generated and to prevent double counting of parameters present in the SPICE model. The design tools at the core of this methodology are Calibre LVS, xCalibrate and Calibre xACT 3D. Figure 1 describes this methodology in detail.

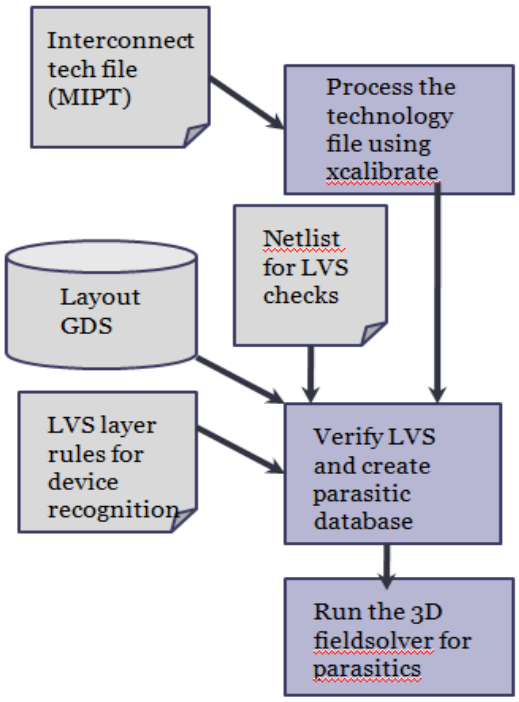

Fig. 1. Methodology for Parasitic Extraction

The following steps further describe the inputs needed by the flow and the important steps in parasitic extraction:

- The layout data of the various bipolar transistors available in the cell library is converted into GDS format and Layout vs. Schematic (LVS) is verified. This involves developing custom SVRF (Standard Verification Rule Format) rules [18] in order to define the layer patterns and connectivity for the given layout.

- The process technology information provided is captured in an interconnect technology file using MIPT 2.0 syntax [6]. We have developed a novel script to parse process technology information and convert it to a custom stack consisting of multiple diffusion and polysilicon layers required to analyze advanced non-planar devices. The MIPT file is then calibrated to generate extraction rules and device definitions for the extraction flow.

- xACT 3D is then invoked which performs the parasitic extraction of the LVS clean data. The tool can be configured to ignore certain capacitances to avoid double counting and to allow us to focus on specific parasitics. We thus generated a capacitance matrix which was used to analyze the fringing fields between specified pairs of layers.

CHAPTER III

ANALYSIS OF FRINGING CAPACITANCE IN MOSFET

The methodology developed in the previous section was first used for a comprehensive analysis of near-device parasitic capacitances in a MOSFET. An advanced process node (65nm) was chosen and the SPICE model provided by Predictive Technology Model (PTM) [7] was used as a reference and for acquiring values of oxide dimensions and dielectric properties. The simulations done using PTM was used primarily to compare the relative contribution of different components of capacitance.

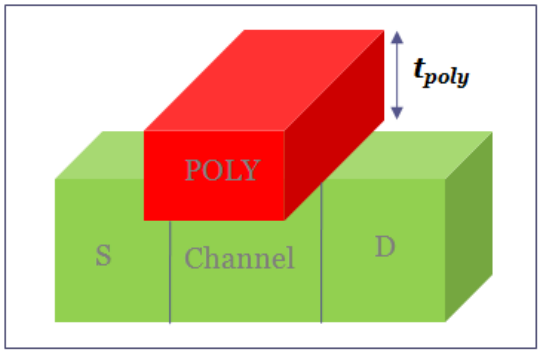

Fig. 2. 3D View of Device Layers in a MOSFET

With the relatively simple geometry of MOSFET, it is easy to understand the effects of 3D geometry on parasitic capacitance. Figure 2 shows a 3D view of a MOSFET and a considerable area of the polysilicon (in red) with height t_{poly} is seen

forming the sidewall. The fields originating from the outer surface of poly sidewall into base diffusion, or the source and drain regions constitutes a good example of fringing field capacitance in MOSFET. These fields combine to form an important parameter of a MOSFET, the gate capacitance. The gate capacitance C_g is the total coupling capacitance between the poly layer (which forms the gate terminal) and the substrate or the diffusion layers (the source and the drain terminals). It is a critical parameter during circuit simulation since it influences a range of other parameters like switching current (I_{on}) and stage delay [3]. Figure 3 shows the important components which form C_g. The components C_{ox} and C_{if} are chiefly controlled by the gate oxide thickness and its dielectric properties and are also bias dependent. As a result, they must be included in the SPICE models. C_{ox} has been modeled based on the operating region of the MOSFET in the BSIM4 model [3] but C_{if} is not included. C_{ov} depends on the amount of overlap between the poly and diffusion layers and is generally included in the SPICE models. Our methodology can be used to extract this parameter in case it is missing. However, we focus on the outer fringing field component C_{of} which is bias-independent and is not included in PTM. C_{of} mainly depends on the relative geometry between the poly and diffusion layers and the shapes of spacer and gate oxides. BSIM has a unit width fringing capacitance parameter CF which can be compared with field solver results.

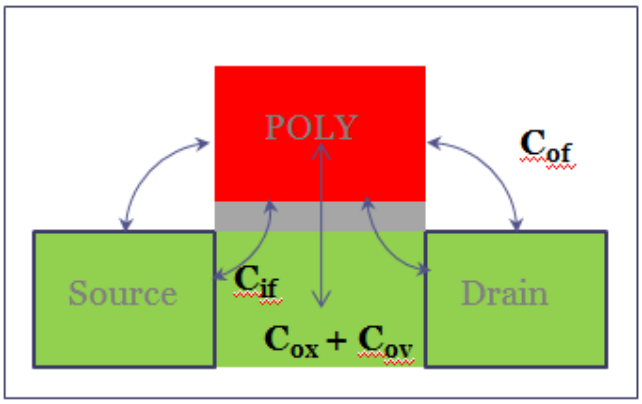

Fig. 3. Gate Capacitance Components in MOSFET

Device Recognition

Device recognition is an important step which serves a dual purpose - verify LVS and construct the device in 3D in conjunction with the interconnect rules. In the case of MOSFET, the layers in the GDS need to be derived in a way which defines the gate, drain and source regions. An important consideration is to separate the poly region into two parts - device poly (the overlap between poly and diffusion) and field poly (the region which extends out of the active diffusion and serves as contact area). This is done in order to analyze the contributions of each separately which is useful in modeling process specific phenomena like bird's beak [8] in which the field poly is at a different plane compared to device poly. The gate oxide layer is also defined as part of the rules as an area between poly and substrate. Table I shows the way in which rules are developed.

Table I. LVS Rule Derivation for MOSFET

MOS Device Recognition	ngate = poly AND active_sized nsd = active_sized NOT poly DEVICE MN(NMOS) ngate ngate(G) nsd(S) nsd(D)
Separate Poly Layers	polycon = poly NOT active_sized CONNECT polycon ngate CONNECT m1 polycon BY contact
Gate Oxide	gate_oxide = COPY ngate

Extraction Results and Analysis

Using the results of 3D field solver extraction, we demonstrate the importance of incorporating geometry effects into the calculation of fringing parasitic capacitance. BSIM4 models the fringing capacitance per unit width parameter *CF* using the following equation:

$$CF = 2.EPSROX.\frac{\varepsilon_0}{\pi}.\log(1+\frac{4e^{-7}}{TOXE})$$

It can be seen that *CF* is modeled with dependencies only on *EPSROX* and *TOXE* (gate oxide dielectric constant and thickness respectively). Deviation from this model is observed when layout specific geometry parameters like dielectric constant of the poly conformal oxide, placement of via relative to poly and via density is taken into account. Figure 4 shows the fringing field lines in more detail. The fringing fields due to field poly is of importance since it is not a function of device width and hence must be modeled separately.

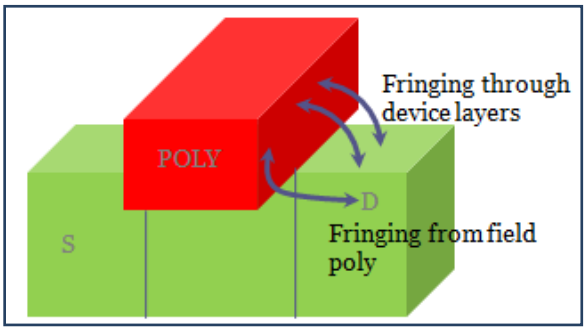

Fig. 4. Fringing Capacitance Divided into Device and Field components

Table II describes the extraction results in detail. C_{of} represents the outer fringing capacitance extracted using xACT 3D and includes the device poly and field poly components. The gate capacitance obtained from SPICE simulation is just the sum of C_{ox} and C_{ov} in the active region of MOS operation. It does not include fringing since it is not modeled in PTM. We have also tabulated the fringing capacitance C_f using the formula provided in BSIM4. The importance of including fringing capacitance is evident since it contributes 20-25% to the total gate capacitance for a range of device widths. As shown in Figure 5, by comparing the extracted C_{of} with the BSIM modeled values of C_f, mismatches can be observed due to the inability of BSIM to model process and geometry related effects like field poly fringing, poly thickness and conformal dielectrics around poly.

Table II. Fringing Capacitance (e^{-16}F) for Various Device Widths

W (*nm*)	C_{of} (xACT)	C_f (BSIM)	C_g (SPICE)
150	0.704	0.179	1.99
200	0.853	0.24	2.69
300	1.185	0.36	4.11
400	1.525	0.48	5.54

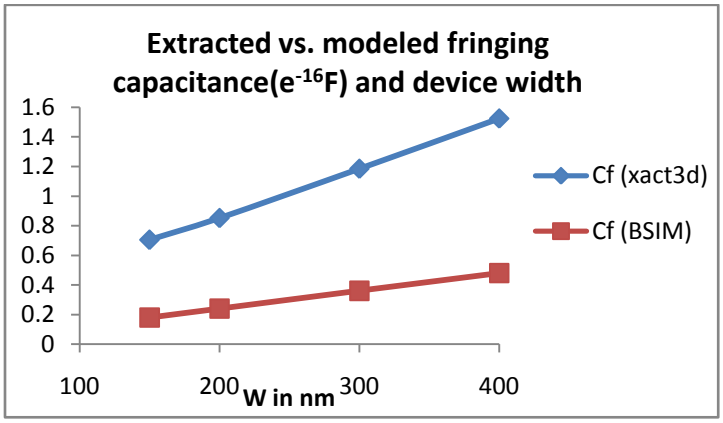

Fig. 5. Comparison of Extracted and Modeled Values of Fringing Capacitance

Via placement is a layout dependent factor which influences the fringing capacitance. The placement of vias on the source/drain (S/D) regions relative to the edge of gate region is analyzed. Extraction results in Figure 6 show that fringing capacitance increases with increasing distance of via from the edge of gate poly layer. Changing the via density on the S/D regions also results in changes in fringing capacitance. Doubling the via density reduced the fringing capacitance between gate and S/D by around 10%.

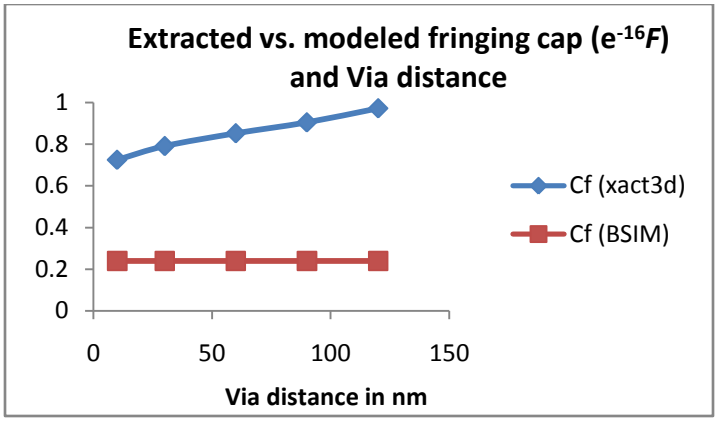

Fig. 6. Comparison of Extracted and Modeled Values of Fringing Capacitance with Varying Via Distance from Gate Edge

The analysis also yielded results on fringing parasitics due to coupling between contact layers and all the base layers (poly and diffusion layers). Due to the proximity of the sidewalls of contacts to the poly layer and considering the relatively large height of contacts, the value of this capacitance dominates the overall C_g. Figure 7 shows the distribution of various components from the extraction reports.

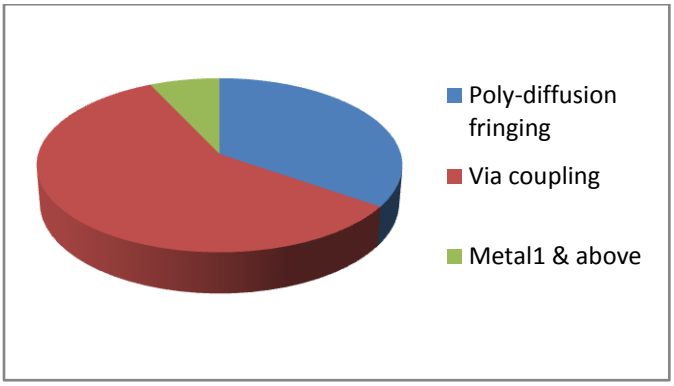

Fig. 7. Contribution of Parasitics due to Contact, Metal and Poly Layers

CHAPTER IV

ANALYSIS OF FRINGING CAPACITANCE IN VERTICAL BJT

A vertical BJT structure is widely used in BiCMOS-based design layouts due to its ability to be packed densely in CMOS-scale process technology [9]. Our study involves a specific kind of vertical BJT which is integrated using a double polysilicon self-aligned process as shown in Figure 8. They offer high density and frequency compared to lateral BJTs due to the scaling down of the emitter area by self-alignment (which reduces the base-emitter junction capacitance) and the ability to fabricate a double-base contact region (which reduces base resistance r_b). However this type of scaling also affects the sidewall spacers which are used to isolate the emitter poly from the base poly. Due to reduction in sidewall oxide spacer thickness, the total base-emitter capacitance is dominated by the peripheral component [10]. The SPICE models do not describe this component sufficiently [11]. Accurate extraction of device parasitic is important because the compact 3D geometry results in large fringing fields and the thin spacer that separates the double poly layers magnifies the fields.

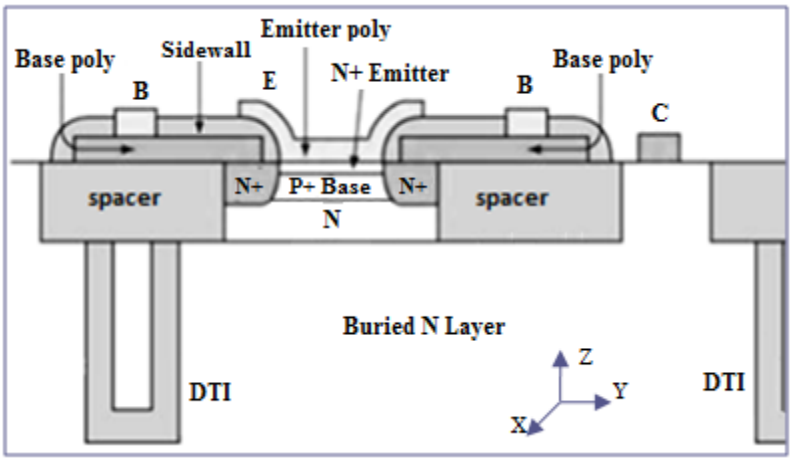

Fig. 8. Vertical BJT Structure (NPN)

The bipolar transistor device model MEXTRAM provided by NXP semiconductors is used as a reference in circuit simulations. It models the base-emitter depletion capacitance (C_{be}) parameter *CJE* as the sum of capacitances on the bottom area of emitter and the sidewall perimeter [11]:

$$CJE = CJE_b.H_e.L_e + CJE_s.2(L_e + H_e)$$

The model only accounts for the junction capacitance and ignores geometry dependent contributions to C_{be}. Figure 9 and Table III describe some important parameters related to the BJT layout which will be used in analysis and modeling.

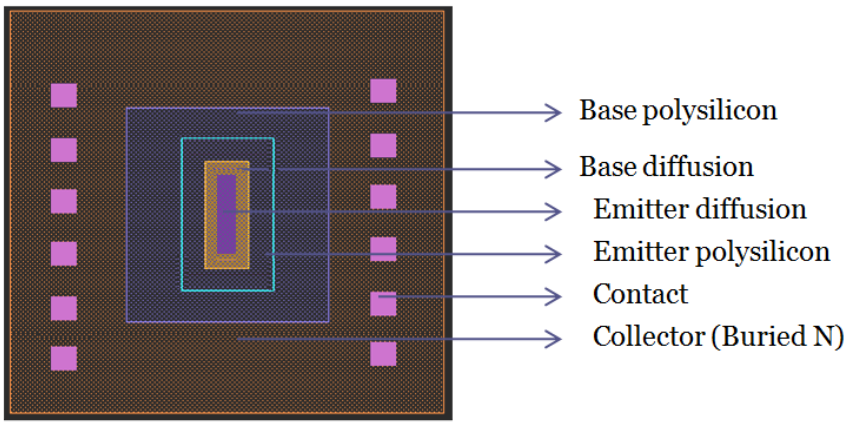

Fig. 9. GDS of Vertical BJT

Table III. Definitions of Layout Parameters of Vertical BJT

Layout Perimeter	Definition
L_e, H_e	Emitter diffusion dimensions
L_b, H_b	Base diffusion dimensions
$A_{e,poly}$, $t_{e,poly}$	Area enclosed by emitter polysilicon and its thickness
$A_{b,poly}$, $t_{b,poly}$	Area enclosed by base polysilicon (larger than $A_{e,poly}$) and its thickness (smaller than $t_{e,poly}$)
t_{sw}	Thickness of oxide spacer between base and emitter
h_{sw}, w_{sw}	Dimensions of oxide spacer around the emitter

Device Recognition

Device recognition in LVS needs the BJT device layers base (B), emitter (E) and Collector (C) and terminals to be generated using Boolean rules which operate on layers. The emitter polysilicon when deposited on a non-planar sidewall spacer results in a characteristic shape which is modeled using multiple thicknesses. This requires multiple

poly layers being described for emitter poly. The base poly overlap of emitter poly is modeled using a mask layer. Layers with the same physical properties are tied together to complete connectivity. Table IV describes in detail the LVS rules used for vertical BJT.

Table IV. LVS Rule Derivation for Vertical BJT

BJT Device Recognition	polye_diff = SIZE polye by *$scale_factor* emitter_diff = SIZE emitter by 0 base_diff = baselayer NOT emitter_diff DEVICE Q(BJT) base_diff collect_diff(C) base_diff(B) emitter_diff(E)
Separate Poly Layers	polye_centre = polye_diff AND emitter_diff polye_connect = polye_diff NOT emitter_diff base_mask = SIZE emitter_diff by *$overlap* polyb_connect = polyb NOT base_mask

Circuit Simulation and Sensitivity Analysis

A circuit designed using BiCMOS was used to test the model and analyze the impact of device parasitics on the overall performance. The circuit employs a delay cell based voltage-controlled oscillator (VCO) design using BJT in differential amplifier configuration as shown in Figure 10 to provide enhanced current drive at the output. On fabrication and testing the circuit was found to have a degradation in frequency compared to the simulated frequency. This was mainly attributed to inaccuracies in

extraction. This methodology was developed as an effort to understand this mismatch and attempt to correct it. Since a field solver based extraction tool is a good fit to analyze device parasitics, we followed a hierarchical approach to extracting the design -

- Standard cells (devices) were identified in the top-level netlist and layout. The device parasitics were extracted separately using xACT 3D.
- The cells were black-boxed in the top-level design and the remaining interconnects were extracted using a conventional LPE tool.
- The cell models were inserted back into the top-level netlist prior to simulation.

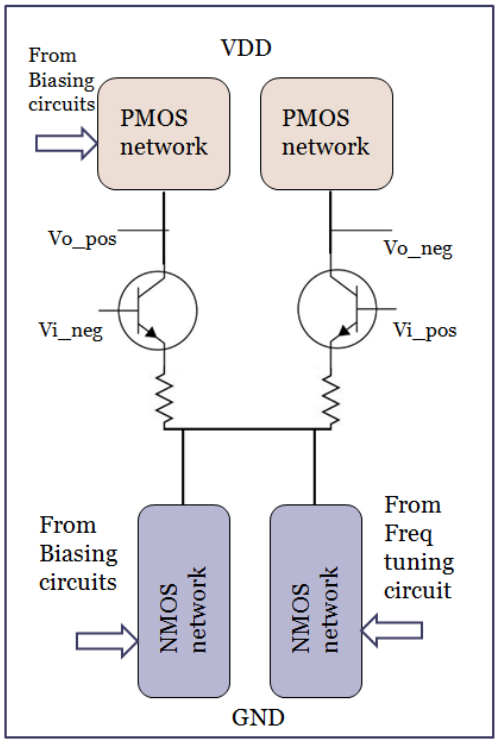

Fig. 10. A Single Delay Cell Used in the Benchmark PLL Design

In order to identify critical nets in a circuit from the extraction point of view, a sensitivity analysis is first performed. We define sensitivity of a particular net or pin as a measure of the change in an observed design metric resulting from a 10% change in total net (or pin) capacitance. Delay cell voltage gain and frequency were the two metrics analyzed in this case. From Figure 11, it can be observed that the inputs signals connected to base (V_i) have more than 2% sensitivity (which is found to be much higher when coupled to the emitter). This points to the importance of the extracted value of C_{be}.

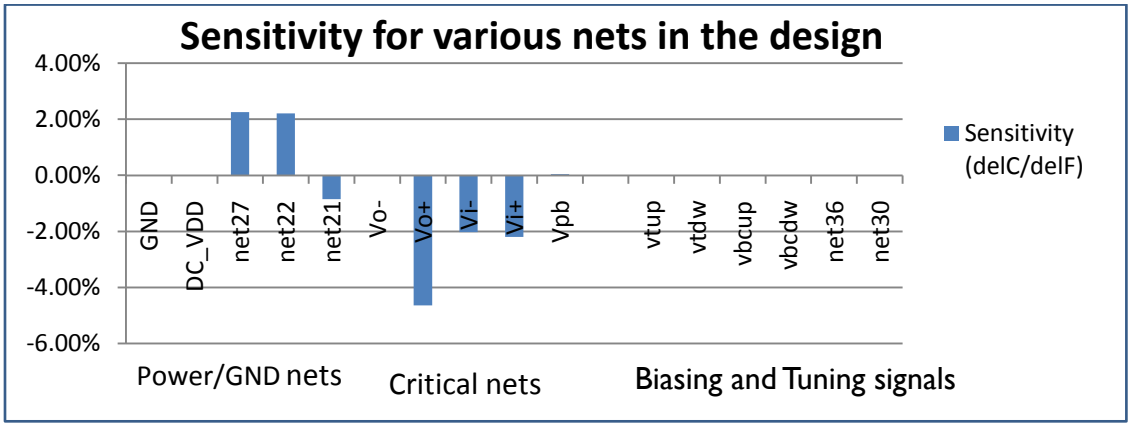

Fig. 11. Sensitivity for Nets in the Delay Cell Design

Extraction Results and Analysis

The total geometry-dependent base-emitter coupling can be expressed as a sum of the following parasitic capacitance components:

- Junction depletion capacitance (C_j)
- Junction fringing capacitance between base and emitter diffusion (C_{jf})

- Fringing fields between base and emitter poly extensions through the spacer sidewall (C_{sw})
- Coupling between the contacts and upper metal layers related to the base and Emitter terminals (C_{ext})

Figure 12 gives a representation of junction capacitance and sidewall capacitance. The sidewall fringing component is expected to dominate since it is sensitive to changes in spacer thickness and needs to be accurately modeled in smaller process nodes.

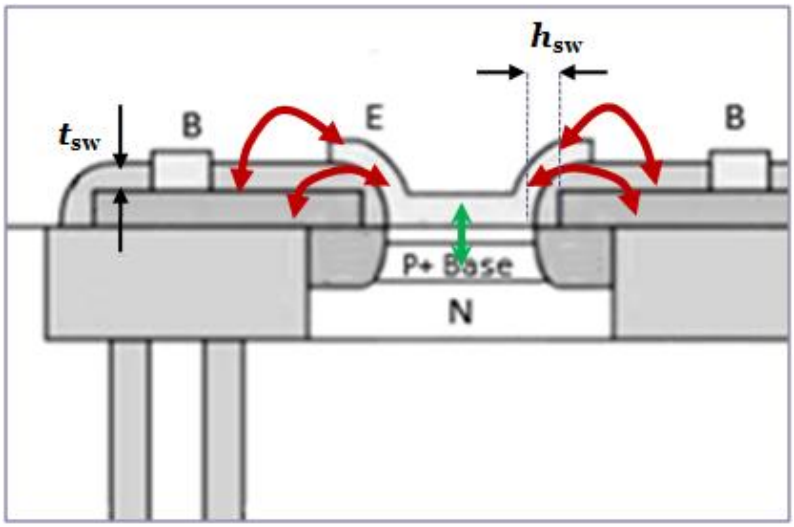

Fig. 12. Junction Capacitance (in Green) and Sidewall Capacitance (in Red)

The device extraction results have been summarized in Figure 13. It can be observed that the sidewall fringing capacitance C_{sw} accounts for a big percentage of total C_{be} and hence needs to be included in circuit simulations. C_{sw} contributes around 53%

of the total base terminal capacitance determined at the bias point. The degradation in observed frequency on silicon can be explained by including this component in SPICE simulations. The fringing fields among contacts and metal layers is dependent on layout styles. For the specific layout used for analysis, it contributed to around 2% of the total base-emitter capacitance. C_{jf} is also determined using the same methodology and was found to be a very small fraction and can be ignored even in lateral BJTs.

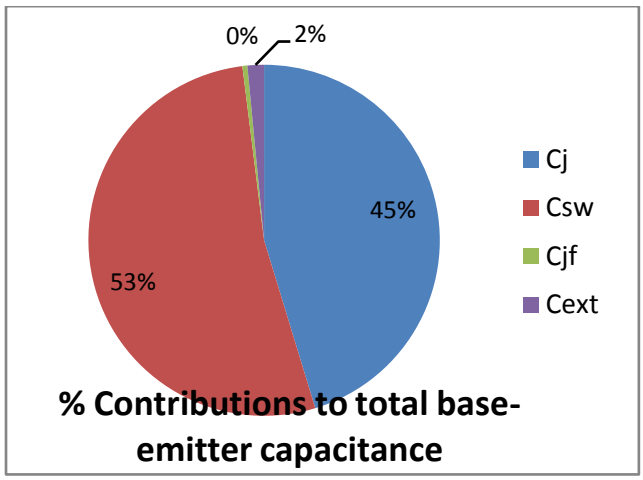

Fig. 13. Various Components of Base-Emitter Capacitance for a Vertical BJT

Table V gives a summary of the benchmarking of the VCO circuit including the extraction methods applied in order to obtain the frequency output from the circuit simulation. LPE 'X' is another rule-based tool which is used along with Calibre xRC to extract parasitics in the circuit. The interconnect process information used for the CMOS devices is the same across all three tools, while the polysilicon data is not supplied to the rule-based LPEs for the BJT devices. Calibre xACT 3D was supplied with typical values

of sidewall spacer dimensions for the given process technology. A degradation of up to 10% in the frequency was observed due to the sidewall fringing parasitics with the 3D field solver based extraction. An exact figure for the frequency could be determined if the interconnect information for sidewall oxide is provided to the flow.

Table V. LPE Tools Used in Benchmarking the BiCMOS Design

	LPE 'X'	**Calibre xRC**	**Calibre xACT 3D**
Extraction Type	Rule-based	Rule-based	3D field solver
Interconnect Stack for CMOS	Diffusion - poly - metal	Diffusion - poly - metal	Diffusion - poly - metal
Interconnect Stack for BJT	Diffusion - metal	Diffusion - metal	Diffusion - double poly - metal and sidewall dimensions
Netlist Type	Flat	Flat	Hierarchical
Diff Amp Gain	2.03	2.03	2.03
VCO Frequency (*GHz*)	2.18	2.18	1.89 to 2.03 (based on a range of t_{sw} values)

Effects of Scaling

Downscaling of the double polysilicon BJT is mainly characterized by the minimum feature sizes of emitter diffusion [12] and thickness of sidewall oxide spacers. This type of scaling is expected to reduce device area and the junction depletion capacitance. Performance gains in terms of current gain and cut-off frequency f_T can be obtained [11] by the scaling of base-emitter depletion capacitance. However, scaling also results in more parasitic capacitances which limits the performance gain [10]. Our

sensitivity analysis also points to a delay impact due to base-emitter parasitics. We thus analyze the impact of scaling when fringing fields are considered.

Figure 14 shows the effect of scaling of emitter perimeter on sidewall fringing capacitance. Although scaling reduces the base-emitter junction capacitance, the fringing capacitance C_{sw} increases which affects the delay of the circuit. Figure 15 demonstrates that downscaling the polyemitter perimeter has no adverse effect on parasitics. Figure 16 shows the inverse relationship between sidewall spacer oxide thickness t_{sw} and sidewall fringing capacitance.

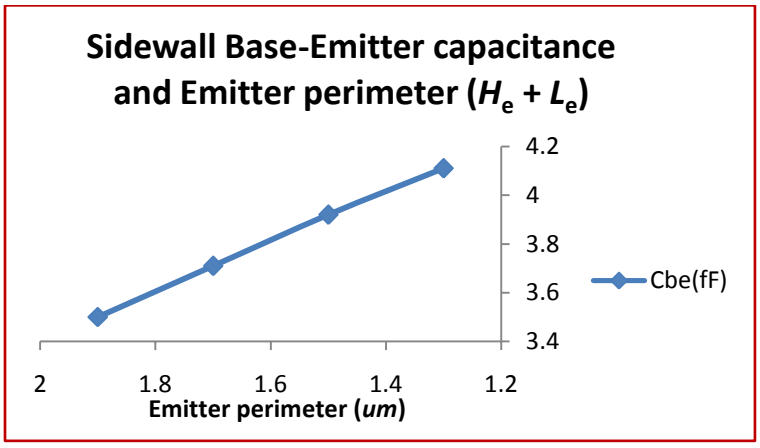

Fig. 14. Sidewall Base-Emitter Capacitance for Various Values of Emitter Perimeter

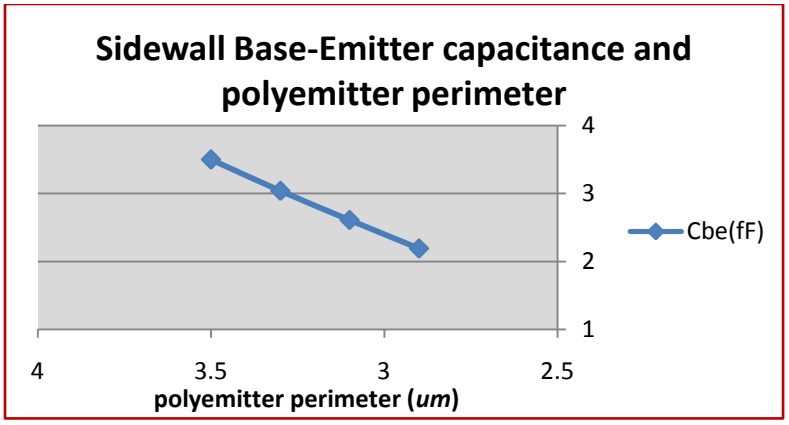

Fig. 15. Sidewall Base-Emitter Capacitance for Various Values of Polyemitter Perimeter

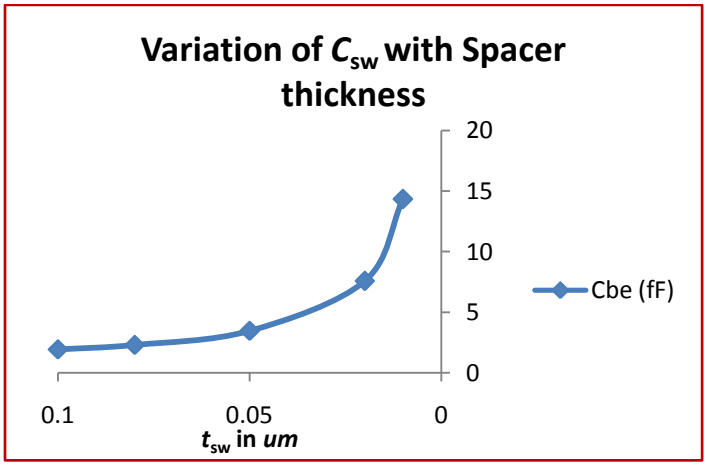

Fig. 16.Variation of Sidewall Capacitance with Spacer Layer Thickness

In order to explain these observations, a model has been developed expressing sidewall parasitic capacitance C_{sw} as a function of base-emitter polysilicon overlap area and emitter diffusion perimeter P_e. An approximation for C_{sw} can be obtained through the following equation:

$$C_{sw} = 0.067 \left(\frac{A_{polyov}}{t_{sw}}\right) + 0.15P_e$$

A_{polyov} is a term which represents the effective overlap between the base polysilicon and emitter polysilicon for the purposes of capacitance modeling. It can be expressed by the following equation:

$$A_{polyov} = A_{e,poly} - (H_e + h_{sw})(L_e + l_{sw})$$

The constants in the equation depend on interconnect process information and are obtained by using curve fitting.

CHAPTER V

ANALYSIS OF FRINGING CAPACITANCE IN FINFET

FinFET devices are characterized by a gate electrode wrapped around a thin fin of diffusion material. Compared to MOSFET devices at the same process node, FinFETs are more attractive due to their ability to control short-channel effects and minimize leakage currents [13]. Accurate extraction of device parasitics is important due to their compact 3D geometry which results in large fringing fields and thin fin structures which cause large S/D resistance [2]. These effects are ignored in the SPICE models and are not sufficiently modeled by conventional 2D LPE tools.

The 45nm FinFET SPICE model available at PTM [7] is used for circuit simulation and gate capacitance calculation. The PTM models the FinFET as a double-gate MOS with two fully depleted SOI transistors, each described using BSIM. The simulations were performed using default values of important parameters ($w = 60nm$; $l = 45nm$, 3 fingers) which yielded a gate capacitance of $0.674fF$ in the active region. The model however ignores the geometry dependent fringing fields and overlap capacitance through the fin hard-mask. Using this as a starting point we analyze the fringing capacitance and its contribution to a circuit built using FinFETs. We present FinFET as an excellent example of how the methodology can be used to characterize the device, analyze the effects of scaling and provide an accurate model for the designer.

The device structure of FinFET is illustrated in Figure 17. Several layout and process parameters can be described in the device structure and the designer has the

flexibility to vary some of these parameters to achieve design goals. Table VI describes these parameters in detail.

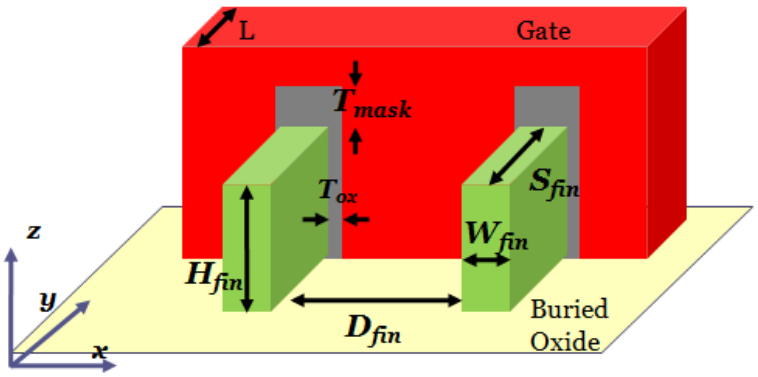

Fig. 17. FinFET Device Structure Using Cross-sectional View

Table VI. Definition of FinFET Layout Parameters

Parameter	Definition
L	Physical gate length as defined by the process technology
W_{fin}	Width of the fin as seen from above
H_{fin} or W	Height of the fin or effectively the width of the FinFET device
T_{ox}	Thickness of gate oxide along the side of the fin
T_{mask}	Thickness of mask hard oxide which covers the top of the fin
D_{fin}	Distance between neighboring fins in multi-finger devices
S_{fin}	The extension of the fin into S/D contact region due to under lapping gate. This portion is enclosed in nitride space

Device Recognition

The 3D field solver methodology developed for the vertical BJT is a good fit to analyze the geometry dependent fringing fields in a FinFET. The inputs are the layout GDS and a sample 45nm interconnect process deck developed using parameters in the PTM as shown in Figure 18.

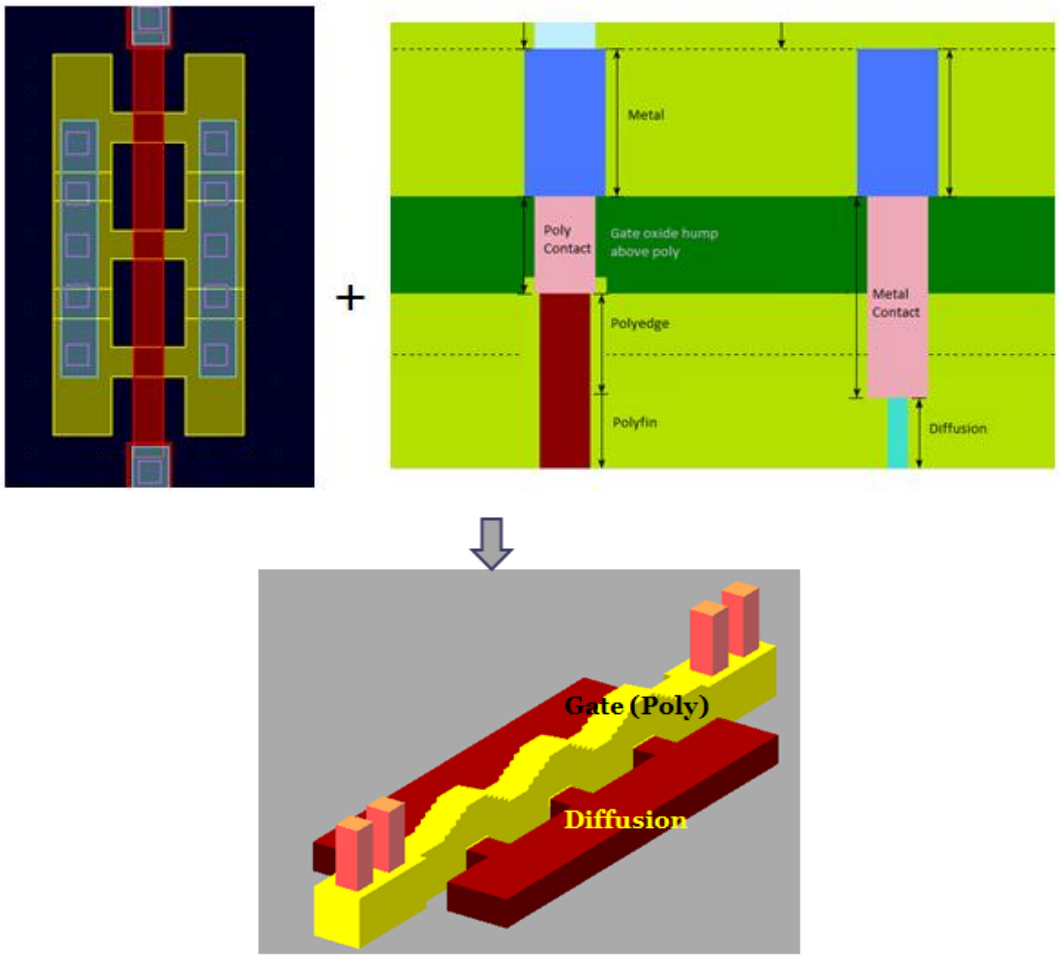

Fig. 18. 3-Dimensional View Generated from GDS and Process Data

Device recognition in LVS requires a regular NMOS/PMOS to be described using a set of Boolean rules. The non-planarity in polysilicon gate electrode is modeled through a step approximation using multiple poly layers with different vertical dimensions in the process stack. The dielectric oxide layers are traced along diffusion or poly layers and provided as mask layers to the extraction tool. Table VII describes in detail the LVS rules used for FinFET.

Table VII. LVS Rule Derivation for FinFET

FinFET Device Recognition	polyfin = poly AND (SIZE active BY *$tox*) nsd = active NOT polyfin DEVICE MN(NMOS) polyfin polyfin(G) nsd(S) nsd(D)
Separate Poly Layers	polystep1 = poly AND ((SIZE polyfin BY 0.005) NOT polyfin) polystep2 = poly AND ((SIZE polyfin BY 0.01) NOT (OR polyfin polystep1)) ... polyside = poly NOT (OR polyfin polystep1 polystep2 polystep3 polystep4) CONNECT polyside polystep1 polystep2 polystep3 polystep4 polyfin
Trace Oxide mask layers	gateoxide = COPY polyfin hardoxide = COPY polyfin nsdoxide = COPY nsd

Circuit Simulation and Sensitivity Analysis

In order to determine the effect of parasitics on delay and circuit performance, a 11-stage ring oscillator circuit was designed using complementary FinFET inverters configured as follows:

$$W_p = 5.(2H_{fin} + W_{fin})$$

$$W_n = 3.(2H_{fin} + W_{fin})$$

The circuit was simulated using the 45*nm* PTM SPICE model with a supply voltage of 1V. With a measured stage delay of 110*ps*, a frequency sensitivity of 6% was observed with changes in gate capacitance.

Extraction Results and Analysis

From a device point of view, the gate electrode is coupled with the substrate, S/D regions, contacts and metal layers. We focus on the gate-to-S/D coupling by ignoring the parasitics due to contacts and metal layers. The gate capacitance consists of the intrinsic gate capacitance C_{ox}, overlap capacitance C_{ov}, inner fringing capacitance C_{if} and outer fringing capacitance C_{of}. C_{ox}, C_{ov} and C_{if} are bias dependent and can be modeled in BSIM or through 2D simulations [14]. The outer fringing component C_{of} is largely bias independent and contributes directly to the total gate coupling. TCAD simulations have shown that even I_{on}/I_{off} characteristics depend on this component [2]. For ease of analysis, C_{of} has been divided into two components:

- The fields which terminate onto the top surface of S/D region ($C_{f,top}$) as shown in Figure 19.
- The fields which terminate onto the side walls of S/D region ($C_{f,sw}$) as shown in Figure 20.

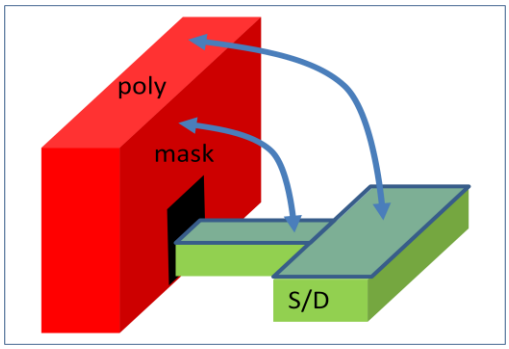

Fig. 19. Field Lines Terminating on the Top Surfaces of Diffusion

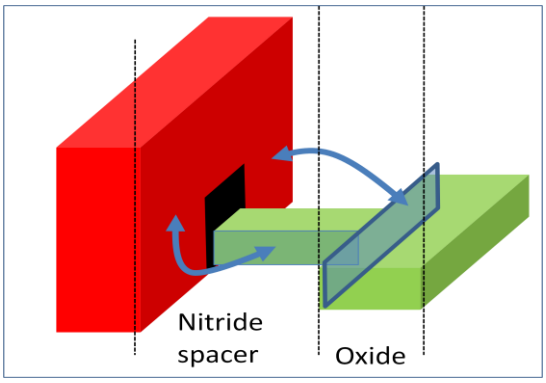

Fig. 20. Field Lines Terminating on the Sidewall Surfaces of Diffusion

Effects of Scaling

In addition to scaling down the gate length and t_{ox} of the actual device, gains can be obtained by scaling down D_{fin} (which reduces device area) and S_{fin} (which improves I_{on}). Our simulations show that scaling D_{fin} reduces the parasitic fringing capacitance, which is a consequence of the reduction of the total sidewall area. This effect is illustrated in Figure 21. Thus D_{fin} can be scaled as much as much as the design rules allow in order to maximize the number of fingers in a given area.

Figure 22 shows the variation of parasitic fringing capacitance with change in S_{fin} keeping D_{fin} constant. By observing the sidewall component, it can be seen that $C_{f,sw}$ degrades at lower dimensions. However, keeping a large value of S_{fin} increases the S/D parasitic resistance. Thus a tradeoff needs to be achieved between these two kinds of parasitics.

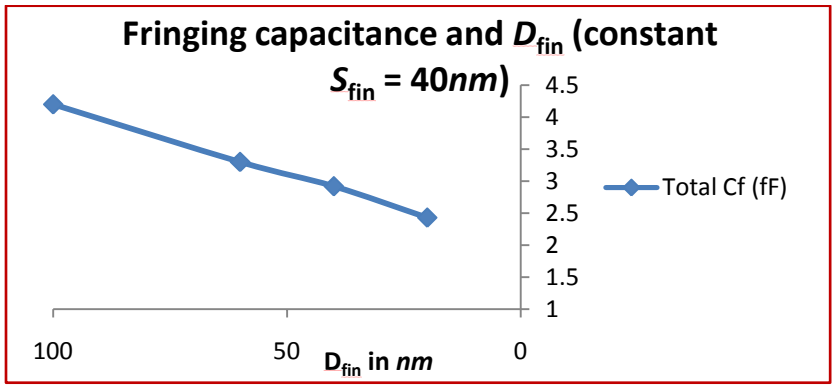

Fig. 21. Fringing Capacitance for Various Values of Distance Between Fins

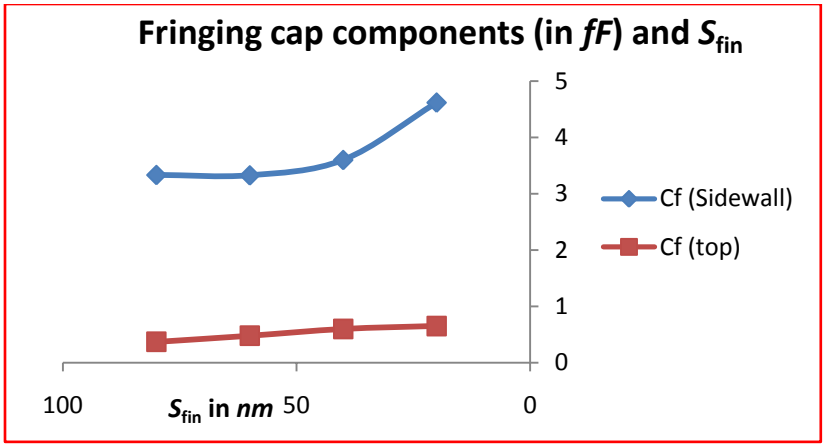

Fig. 22. Fringing Capacitance of Sidewall and Top Surface Components for Various Fin Extensions

Modeling of Raised Gate in Nanoscale FinFET

Nanoscale fabrication methods for FinFETs result in a raised profile for the gate electrode around the fin region [15]. The standalone effects of the raised-gate has largely been ignored in works involving TCAD simulations. Results based on field solver based extraction show that total fringing capacitance is very sensitive to changes in thickness of poly layer, specifically the area of the sidewall. The gate-hump can be modeled for parasitic extraction using a step-approximation as shown in Figure 23 which closely follows the curve function provided by the process or foundry. In addition to approximating the raised gate, this approach can also be used to model the epitaxial raised source/drain (RSD) in high-performance FinFETs [16]. The step approximation would be a good fit for analyzing fringing fields due to the trapezoidal profile of RSD.

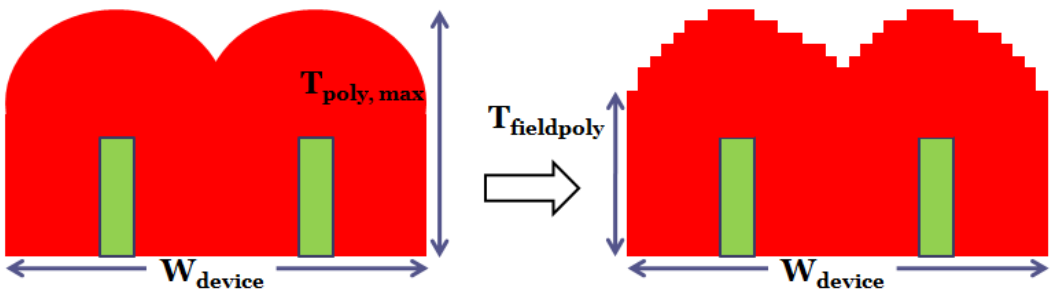

Fig. 23. Step Approximation of the Raised Gate Layer

Using the step approximation places a larger accuracy requirement on the field solver which increases the run-time. Thus a model for a planar polysilicon layer is presented. By extracting devices over a range of acceptable values of D_{fin} and S_{fin} [17] we have observed that an approximation can be obtained by analyzing two different cases involving the relative values of D_{fin} and S_{fin}. The two cases are as follows:

- When the extension of the fin is larger than distance between neighboring fins ($S_{fin} > D_{fin}$), matching can be obtained by calculating the effective area of the sidewall poly. The poly can be replaced by a planar layer with effective thickness T_{poly}. Given W_{device} as the effective device width as measured by the product of the number of fins and D_{fin}, T_{poly} can be calculated using the following equation:

$$\int_0^{W_{device}} t_{poly}(x)\,dx = \sum_0^{W_{device}} t_{polyi} * x_i = T_{poly} * W_{device}$$

- When the extension of the fin is smaller than distance between neighboring fins ($S_{fin} < D_{fin}$), the S/D sidewall fringing capacitance dominates the total fringe capacitance. Using the equivalent thickness overcompensates this component.

Hence poly thickness can be taken as $T_{fieldpoly}$ which is the thickness of field poly used for via connections.

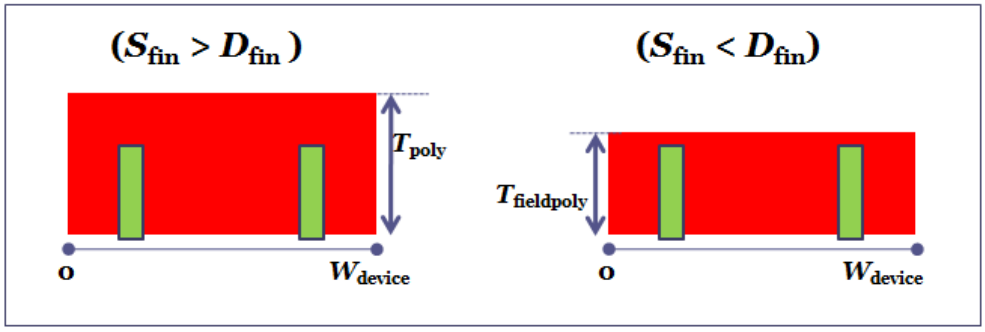

Fig. 24. Modeling Fringing Capacitance Using Planar Polysilicon Layers

The two cases are illustrated in Figure 24. Table VIII demonstrates the accuracy of modeling the raised gate using planar polysilicon using a sample layout with D_{fin} = 60nm. The extraction is performed for a range of values of S_{fin} in typical FinFETs. Assuming that the parasitics obtained using step approximation to be the most accurate, the maximum error in planar poly modeling is less than 2% over the range of devices extracted. The highlighted values represent the parasitics closest to the step approximation. Table IX shows similar results for D_{fin} = 40nm.

Table VIII. Comparison of Step Approximation and Planar Poly Layer Modeling (D_{fin} = 60nm)

S_{fin} (*nm*)	C_f with step	C_f using $T_{fieldpoly}$	C_f using T_{poly}
80	2.53	2.69	2.56 ✓
60	2.67	2.76	2.69 ✓
40	2.89	2.87 ✓	2.98
20	3.47	3.43 ✓	3.39

Table IX. Comparison of Step Approximation and Planar Poly Layer Modeling (D_{fin} = 40nm)

S_{fin} (*nm*)	C_f with step	C_f using $T_{fieldpoly}$	C_f using T_{poly}
80	2.21	2.43	2.19 ✓
60	2.36	2.5	2.40 ✓
40	2.62	2.68	2.66 ✓
20	3.15	3.21 ✓	3.02

CHAPTER VI

CONCLUSIONS

A robust methodology for the analysis of parasitic capacitances using a 3D field solver based extraction tool has been presented. It provides for a convenient way of modeling parasitic capacitances in advanced nanoscale devices by extracting layout geometry and combining it with the interconnect process information. The flow offers the following benefits -

- The inputs provided to the flow is similar to any conventional extraction tool. Accurate 3D views are generated by using the layout GDS and process information.
- Device and layer recognition using Calibre LVS enables detailed layer-to-layer capacitance calculations which is critical in the analysis of nanoscale devices.
- The basic templates for CMOS, vertical BJT and FinFET have been developed as part of this study. Designers can make use of these to develop models for various other geometries.
- The run time obtained using the 3D field solver is much smaller compared to device simulators. The analysis of a FinFET cell on an AMD Opteron (2.2GHz) workstation at maximum grid resolution takes less than 1 minute.

- The flow provides higher accuracy compared to model based analysis like BSIM and accounts for variations in layout geometry like via placement and use of local interconnect.

Because of the close relationship between layout and process technology, the effects of technology scaling can be analyzed. This type of analysis can be used to determine the effects of various parameters on parasitics and the overall performance of the device. The circuit analysis of vertical BJT demonstrates good silicon correlation for the parasitics obtained using the extraction methodology.

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VITA

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